AXM8171A-250

Digital Class-D Audio Amplifier Module

DESCRIPTION

The AXM8171A-250 is a mono digital Class-D audio amplifier module. It features extremely low power losses and exceptional audio performance. The device is packaged in a metal-cased through-hole module (35mmx45mmx12.5mm) (PCB to top of casing).

A digital audio input allows for easy interfacing with streaming services and other digital formats without requiring an external digital-to-analog converter (DAC). The digital architecture eliminates the need for any form of pre-amplification and retains the signal integrity of the audio in the digital domain.

Using post-filter feedback, this class-D audio amplifier retains excellent audio quality for all audio frequencies and signal amplitudes. The frequency response of the system is completely flat (<0.05dB deviation up to 20kHz) in the audio band and load-independent.

The AXM8171A is available in four versions with different power levels:

- AXM8171A-50: 50W/4Ω or 25W/8Ω
- AXM8171A-100: 100W/4Ω or 50W/8Ω
- AXM8171A-150: 150W/4Ω or 75W/8Ω
- AXM8171A-250: 250W/4Ω or 125W/8Ω

FEATURES

- Digital Audio Input:
  - Configurable I²S and Time Division Multiplexing (TDM) Input Formats
  - Configurable Input Sample Rate
- High Efficiency:
  - 92% Efficiency at Rated Power (4Ω)
- Low Losses and Cooler Thermals:
  - 2W Idle Loss
- Excellent Audio Quality:
  - 117dB(A) Dynamic Range
  - THD + N < 0.005%, 4Ω, 20Hz to 20kHz
  - High-Resolution Frequency Response (20Hz to 40kHz)
- Protection Features:
  - Integrated Over-Current Protection (OCP), Over-Temperature Protection (OTP), Under-Voltage Protection (UVP), Over-Voltage Protection (OVP), DC Protection, and Loss of Clock Protection
- Flexible Control Interface:
  - I²C Target Interface or Hardware Pin Control

APPLICATIONS

- Home Audio
- Monitor Speakers
- Custom Installations

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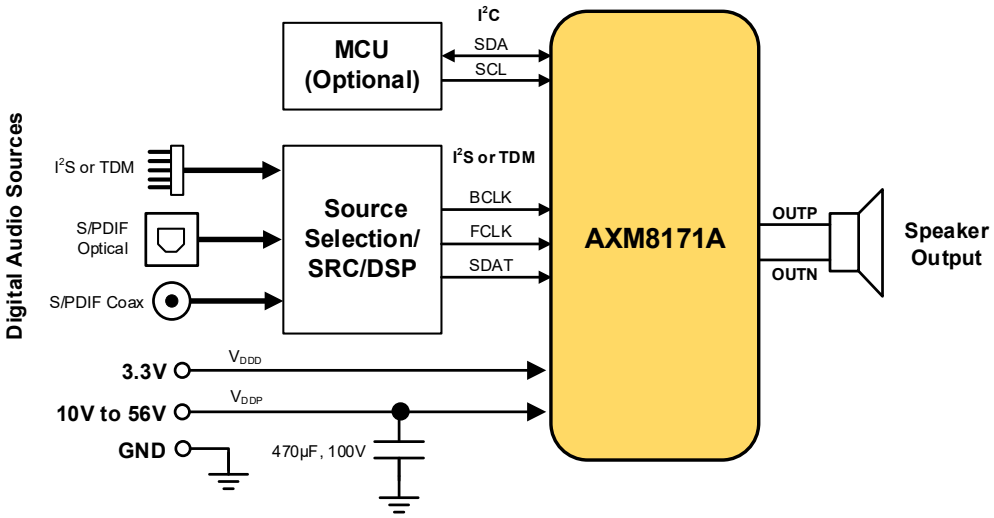
TYPICAL APPLICATION



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ORDERING INFORMATION

Part Number*	Package	Bottom Marking	MSL Rating
AXM8171A-250	35mmx45mm	*See Below*	N/A
DXM8171A-001	Evaluation kit		

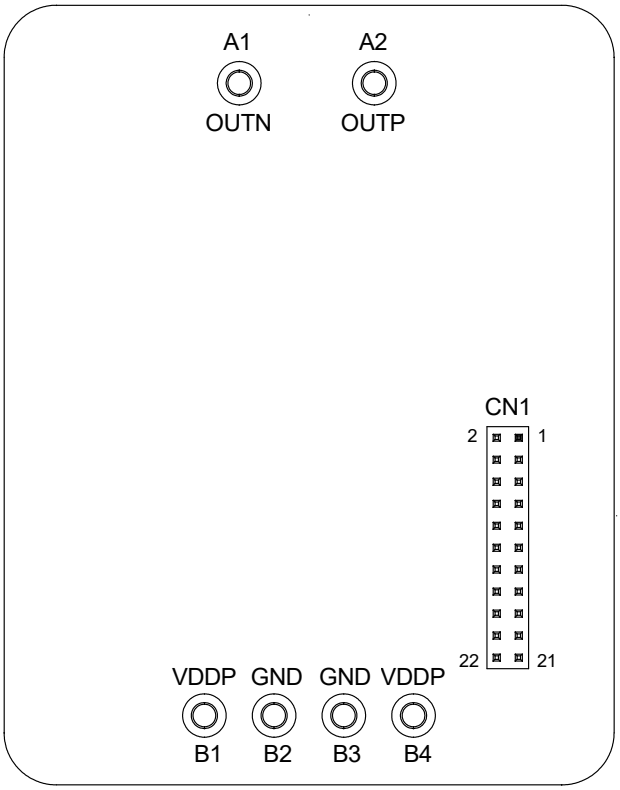
BOTTOM MARKING

AXM8171A-
PPP
LLLLLLLLLLL
YYWWSSSSSSS

AXM8171A: Part number
PPP: Output power level
LLLLLLLLLLL: Lot number
YY: Year code
WW: Week code
SSSSSSS: Serial number

PACKAGE REFERENCE

TOP VIEW



35mmx45mm

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PIN FUNCTIONS

Pin #	Name	Description
A1	OUTN	**Negative output.** Connect the OUTN pin to the speaker.
A2	OUTP	**Positive output.** Connect the OUTP pin to the speaker.
B1, B4	VDDP	**Amplifier power supply.** Connect the VDDP pin to the 10V to 56V power supply, where the required voltage depends on the module's output power (P_{OUT}). Connect a 220µF electrolytic capacitor to ground.
B2, B3	GND	**Ground.**
Connector CN1		
1, 19	VDDD	**3.3V power supply.** Place a 100µF electrolytic capacitor between VDDD and ground.
3, 6, 13, 15, 17	GND	**Ground.**
16	SDI	**Serial I^2S audio data input.**
18	BCLK	**Serial I^2S audio bit clock input.**
20	FCLK	**Serial I^2S audio frame clock input.**
2	nRESET	**Reset input.** Pull the nRESET pin active low to reset the module. nRESET has an internal pull-up resistor.
7	HW/SW	**Control mode selection.** The HW/SW pin is low for HW mode, and the pin is high for SW mode. HW/SW has an internal pull-up resistor.
8	I2S/TDM	**Input mode selection (HW mode only).** The I2S/TDM pin is low for the I^2S stream, and the pin is high for time division multiplexing (TDM) mode. I2S/TDM has an internal pull-up resistor.
4	SR0	**Sample rate selection 0 (HW mode only).** The SR0 pin selects the input sample rate. SR0 has an internal pull-up resistor.
14	SR1	**Sample rate selection 1 (HW mode only).** The SR1 pin selects the input sample rate. SR1 has an internal pull-up resistor.
12	SR2	**Sample rate selection 2 (HW mode only).** The SR2 pin selects the input sample rate. SR2 has an internal pull-up resistor.
9	ADR0	**I^2C address pin 0 or I2S/TDM slot 1.** The ADR0 pin selects the I^2C target address (SW mode) or I^2S/TDM slot (HW mode).
11	ADR1	**I^2C address pin 1 or I2S/TDM slot 2.** The ADR1 pin selects the I^2C target address (SW mode) or I^2S/TDM slot (HW mode).
21	SDA/ON	**Serial I^2C data or on/off control.** The SDA/ON pin sets the I^2C interface for module control (SW mode) or the module's on/off control (where SDA/ON must be pulled high to turn the module on) (HW mode). SDA/ON has an internal pull-up resistor.
22	SCL/MUTE	**Serial I^2C clock or mute.** The SCL/MUTE pin sets the I^2C interface for module control (SW mode) or mute (where SCL/MUTE must be pulled low for the mute function) (HW mode). SCL/MUTE has an internal pull-up resistor.
5	TEST1	**Reserved for testing.**
10	TEST2	**Reserved for testing.**

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ABSOLUTE MAXIMUM RATINGS (1)

Supply voltage (V_{DDD}).....-0.3V to +3.6V
Supply voltage (V_{DDP}).....-0.3V to +60V
Output voltage (V_{OUTx}) ……
……..-0.3V to V_{DDP} + 0.6V
All other pins ..... -0.3V to V_{DDD} + 0.3V
Lead temperature .....260°C
Continuous power dissipation (T_A = 25°C) (2)
..... 10W
Junction temperature (T_J) .....150°C

ESD Ratings

Human body model (HBM) 2000V
Charged-device model (CDM).....750V

Recommended Operating Conditions (3)

Supply voltage (V_{DDP})..... 10V to 56V
Supply voltage (V_{DDD}).....3.1V to 3.6V
Operating ambient temp (T_A) ..... -40°C to +85°C
Load impedance .....2Ω to ∞Ω
Load capacitance..... 0nF to 330nF

Thermal Resistance

Junction-to-case resistance ($R_{\theta JC}$)..... 5.53K/W
Junction-to-ambient resistance ($R_{\theta JA}$).....
……...12.42K/W

Notes:

1) Exceeding these ratings may damage the device.
2) Exceeding the maximum allowable power dissipation can produce an excessive module temperature, and the amplifier may go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) The device is not guaranteed to function outside of its operating conditions.

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ELECTRICAL CHARACTERISTICS

V_{DDP} = 48V, V_{DDD} = 3.3V, T_A = 25°C, R_{LOAD} = 4Ω, fs = 96kHz, I^2S, unless otherwise noted.

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Power Supply						
VDDP input voltage range			10	48	56	V
VDDP pin voltage (V_{DDP}) over-voltage lockout (OVLO)				58		V
V_{DDP} under-voltage lockout (UVLO)				9		V
VDDP supply current		Output muted		23		mA
		Output off		680		µA
		Full-rated power, R_L = 4Ω		5.6		A
		Full-rated power, R_L = 4Ω (5)		11		A_{PEAK}
		Full-rated power, R_L = 8Ω (5)		3		A
		Full-rated power, R_L = 8Ω (5)		5.5		A_{PEAK}
VDDP power supply rejection ratio (PSRR) (5)		20Hz to 5kHz		90		dB
		20Hz to 20kHz		70		dB
VDDD input voltage range			3.1	3.3	3.6	V
VDDD supply current		Output unmuted	173	188	211	mA
Digital Input Pins						
Input logic low threshold (5)	V_{IL}				1	V
Input logic high threshold (5)	V_{IH}		2.1			V
Internal pull-up resistance		To V_{DDD}		10		kΩ
Audio Specifications (4)						
Frequency response		-2dB	20		40k	Hz
Gain			65	68.5	71	V_{RMS}/FS
Idle noise		20Hz to 20kHz, A-weighted		42	75	μV_{RMS}(A)
DC output offset voltage			-10	0	10	mV
THD + N		100W/4Ω, 20Hz to 20kHz		0.005	0.02	%
IMD (CCIF) (5)		100W/4Ω		0.0016		%
Dynamic range			112.6	117.6		dB(A)
Rated power output		R_L = 4Ω, -6dB FS		250		W
		R_L = 8Ω, -6dB FS (5)		125		W
Output impedance (5)		20Hz to 20kHz			400	µΩ
		DC to 1kHz			40	µΩ
Efficiency (5)		Full-rated power, R_L = 4Ω		92		%
Idle loss		No signal, V_{DDP} = 48V		2		W
Switching frequency (5)		BD modulation		614		kHz
Timing Characteristics						
Start-up time (5)	t_{ON}	HW mode (hardware control), SDA/ON and SCL/MUTE are pulled high, time from applying V_{DDD} and V_{DDP} until first audio		800		ms

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ELECTRICAL CHARACTERISTICS *(continued)*

V_{DDP} = 48V, V_{DDD} = 3.3V, T_A = 25°C, R_{LOAD} = 4Ω, fs = 96kHz, I^2S, unless otherwise noted.

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Restart time (5)	t_{RES}	Restart time after over-current protection (OCP)/over-temperature protection (OTP)		100		ms
Device Protections						
Output DC offset protection threshold (5)				2		V
Output current limit (5)				20		A
Over-temperature (OT) warning (5)		Junction temperature		125		°C
OT threshold (5)		Junction temperature		150		°C

Notes:

4) Measured at the module output terminals, A1 and A2.
5) Not production tested.

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I²C TIMING CHARACTERISTICS (6)

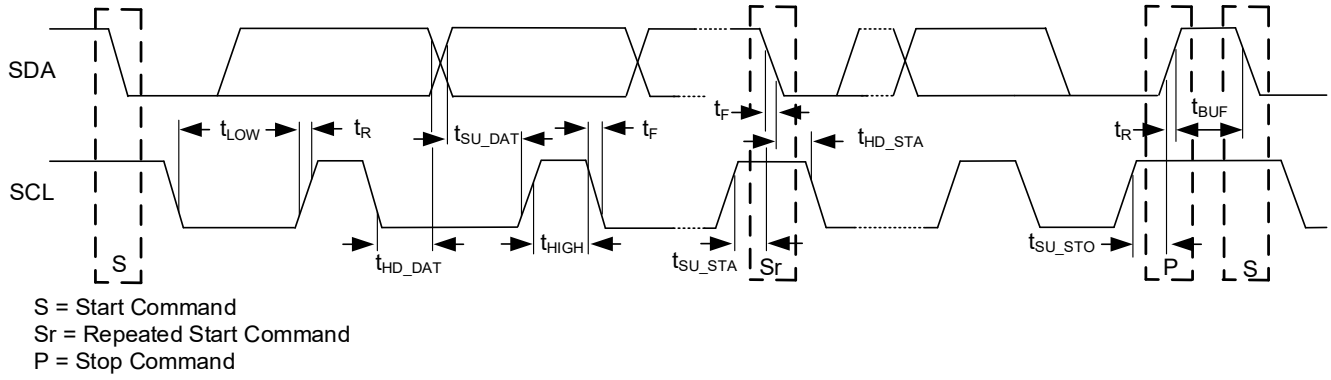
V_{DDD} = 3.3V, T_A = 25°C, unless otherwise noted.

Parameter	Symbol	Conditions	Min	Typ	Max	Units
SCL clock frequency	f_{SCL}		10		500	kHz
Bus free time	t_{BUF}	Between stop and start commands	0.5			µs
Holding time after repeated start command	t_{HD_STA}	After this period, the first clock is generated	0.26			µs
Repeated start command set-up time	t_{SU_STA}		0.26			µs
Stop command set-up time	t_{SU_STO}		0.26			µs
Data hold time	t_{HD_DAT}		0			ns
Data set-up time	t_{SU_DAT}		50			ns
Clock low time	t_{LOW}		0.5			µs
Clock high time	t_{HIGH}		0.26		50	µs
Clock/data falling time	t_F				120	ns
Clock/data rising time	t_R				120	ns

Note:

6) Not subject to production testing. Specified by design.

I²C TIMING DIAGRAM



S = Start Command
Sr = Repeated Start Command
P = Stop Command

Figure 1: I²C Timing Diagram

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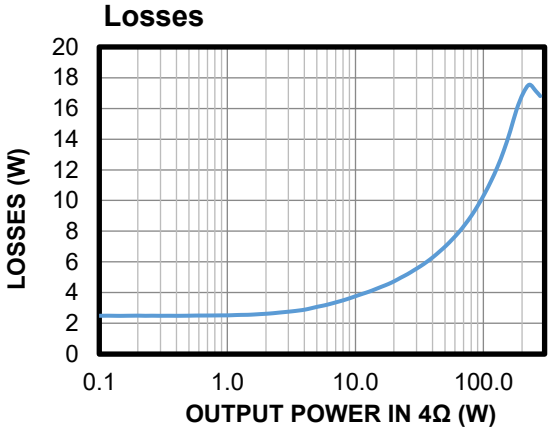
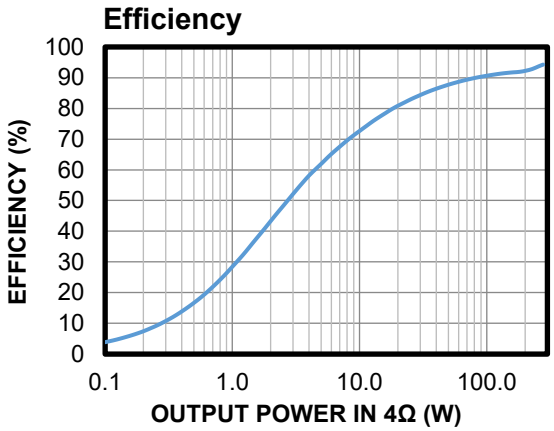
TYPICAL CHARACTERISTICS

V_{DDP} = 48V, V_{DDD} = 3.3V, T_A = 25°C, R_{LOAD} = 4Ω, fs = 96kHz, I^2S, unless otherwise noted.





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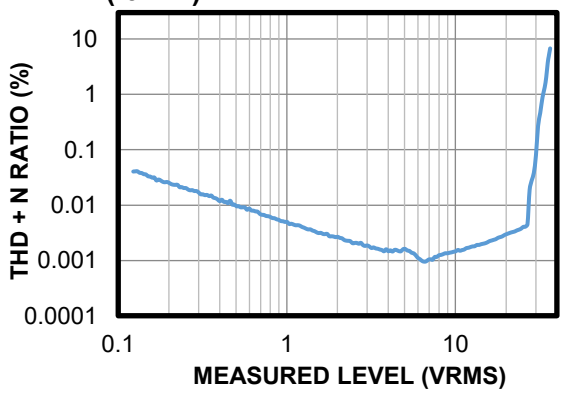
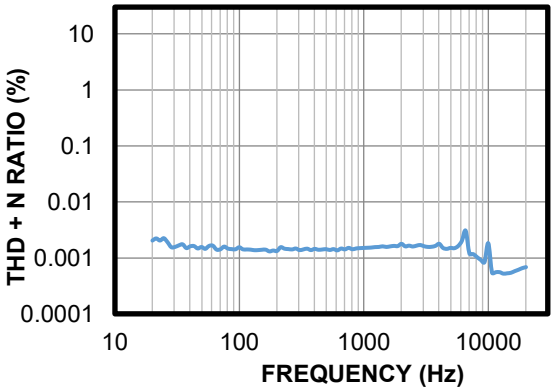
TYPICAL PERFORMANCE CHARACTERISTICS

V_{DDP} = 48V, V_{DDD} = 3.3V, T_A = 25°C, R_{LOAD} = 4Ω, fs = 96kHz, I^2S, unless otherwise noted.

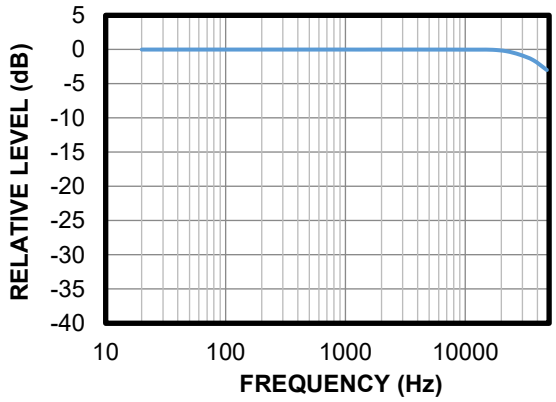
THD+N Ratio vs Measured Level (6kHz)



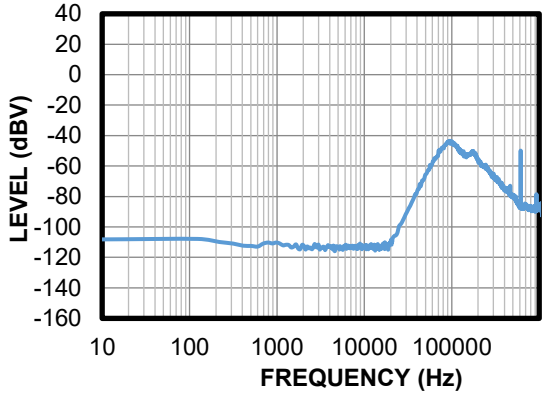
THD+N Ratio vs Frequency (50W)



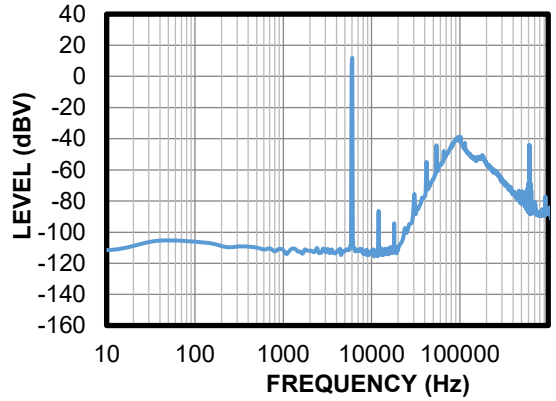
Relative Level (1 kHz)



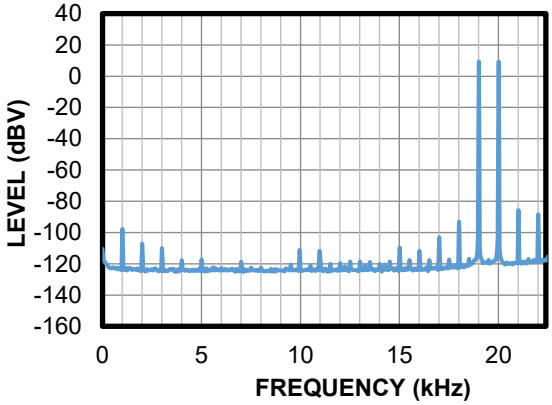
FFT Spectrum



FFT Spectrum 6kHz



FFT Spectrum IMD 5W



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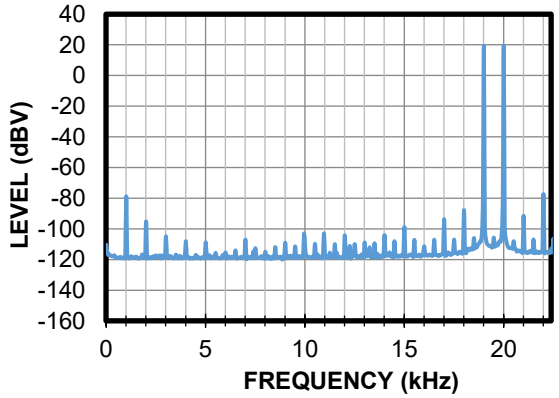
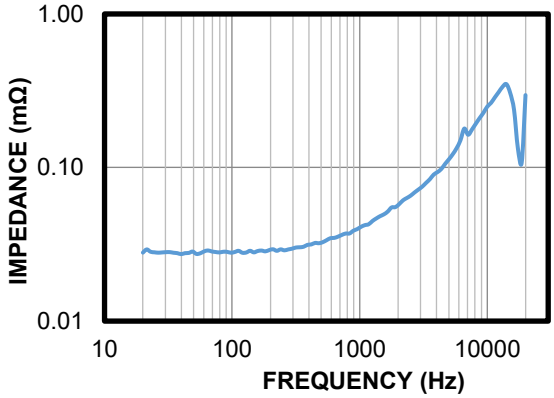
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{DDP} = 48V, V_{DDD} = 3.3V, T_A = 25°C, R_{LOAD} = 4Ω, fs = 96kHz, I^2S, unless otherwise noted.

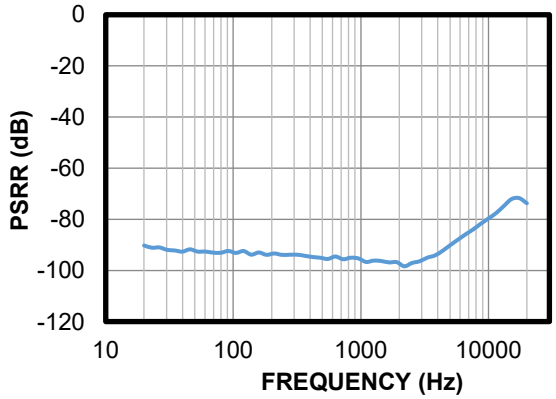
FFT Spectrum IMD 50W



Output Impedance



PSRR



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FUNCTIONAL BLOCK DIAGRAM

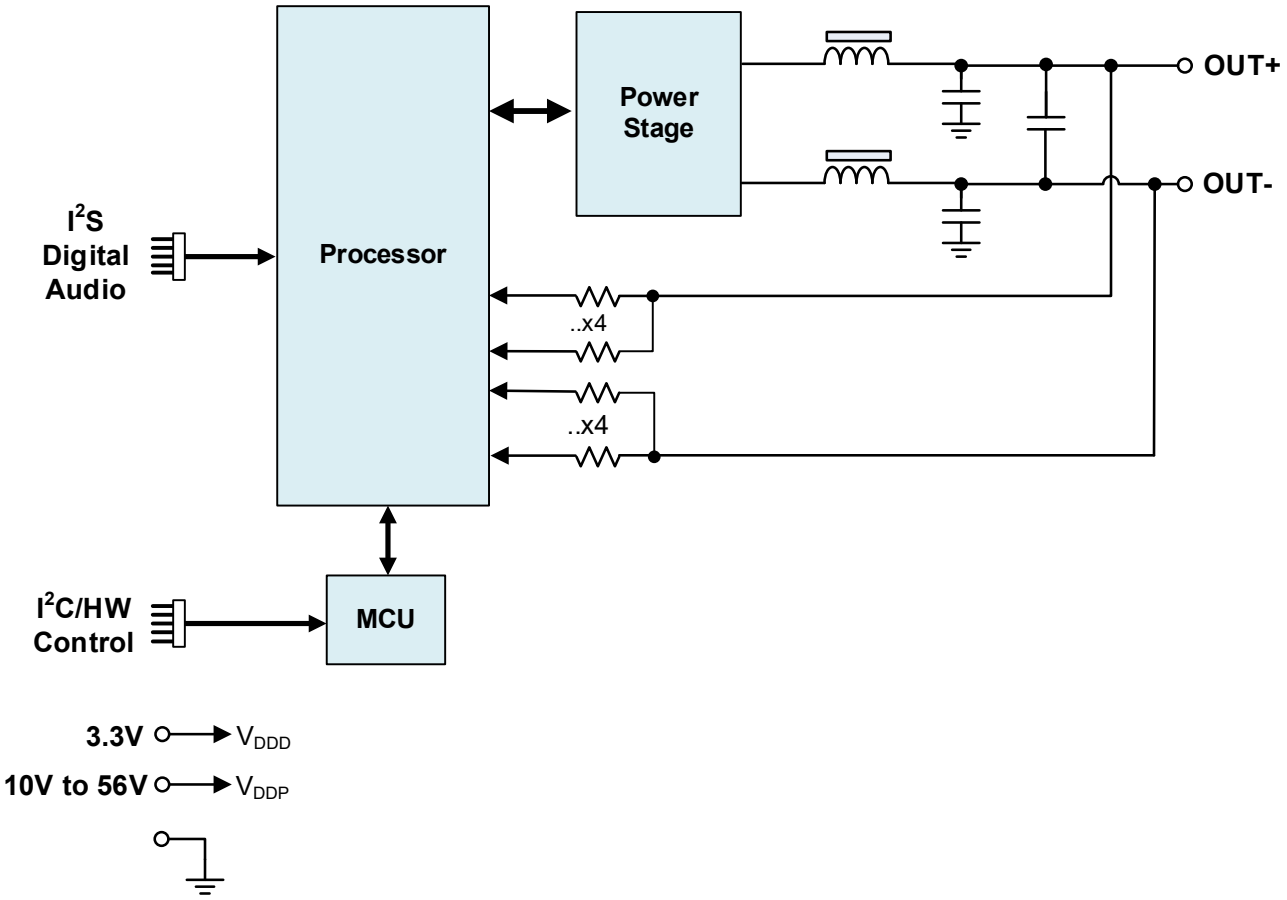

Figure 2: Functional Block Diagram

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OPERATION

The AXM8171A-250 is a complete class-D audio amplifier module. The device operates from a 10V to 56V DC power supply input, and can supply 250W into a 4Ω load or 125W into an 8Ω load.

The AXM8171A module is based on an Axign digital class-D amplifier processor. An Axign power stage drives the speaker through an integrated output filter, implementing a complete digital class-D amplifier.

The audio input to the AXM8171A is in digital I^2S or time division multiplexing (TDM) format. A control interface enables configuration options, such as the input data format, mute, and gain correction.

Module Connections

There is a connector used for control (CN1), as well as 6 large pins on the AXM8171A. The pins can be soldered directly into the host motherboard or connected to a mating socket. For more details, see the Application Information section on page 15.

CN1 is used for the digital audio input and the control interface, which are all low-level signals. This connector uses a 1.27mm pitch and a 11-pin, 2-row header.

The other pins carry the power input, ground, and audio outputs. Large pins are used to accommodate the required current. The pins are 1.5mm in diameter.

Control Interface

The AXM8171A can be controlled either via the hardware pins (HW mode) or via a target I^2C interface (SW mode). The interface allows direct control of module features. In HW mode, no microcontroller is required to use the AXM8171A.

All interface pins have internal pull-up resistors to VDDD. Table 1 shows the CN1 pin functions.

Table 1: CN1 Pin Functions

CN1 Pin #	Pin Name	Function in HW Mode	Function in SW Mode
9	ADR1	I^2S or TDM slot selection	I^2C address MSB
11	ADR0		I^2C address LSB
7	HW/SW	HW or SW mode selection. If the HW/SW pin is low, the device enters HW mode.	HW or SW mode selection. If the HW/SW pin is low, the device enters HW mode.
8	I2S/TDM	I^2S or TDM input mode selection. If the I2S/TDM pin is low, the device selects I^2S input mode.	Unused
4	SR0	Sample rate selection pin 0	Unused
14	SR1	Sample rate selection pin 1	Unused
12	SR2	Sample rate selection pin 2	Unused
21	SDA/ON	Module on/off. If the SDA/ON pin is low, the module turns off.	I^2C data
22	SCL/MUTE	Mute. If the SCL/MUTE pin is pulled low, the mute function is enabled.	I^2C clock

Hardware Control (HW Mode)

When set for hardware control, the pins on CN1 are used to set module functions. Hardware mode is enabled by setting the HW/SW pin to logic low.

In hardware mode, the digital audio configuration and the input sample rate are set by pins. Table 2 on page 13 shows digital HW mode selection, and Table 3 on page 13 shows the HW mode sample rate selection.

The HW mode control pins should only be changed when the module is off; otherwise, unstable operation may result.

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Table 2: Digital HW Mode Selection

Configuration	ADR1	ADR0	I2S/TDM
I²S left	0	-	0
I²S right	1	-	0
TDM4 slot 1	0	0	1
TDM4 slot 2	1	0	1
TDM4 slot 3	0	1	1
TDM4 slot 4	1	1	1

Table 3: HW Mode Sample Rate Selection

Sample Rate	SR0	SR1	SR2
44.1k	0	0	0
48k	0	0	1
88.2k	0	1	0
96k	0	1	1
176.4k	1	0	0
192k	1	0	1

In addition to these settings, the module's on/off and mute functions are controlled via the pins.

I²C Control (SW Mode)

Four I²C addresses can be selected using the ADR0 and ADR1 inputs. Pull ADR0 and ADR1 high or low to set the module's target address. As a result, four different addresses are supported, allowing up to four modules to be addressed using a single I²C interface.

The ADR1 and ADR0 pins have no internal pull-up or pull-down resistors. Connect ADR1 and ADR0 to ground to set them to 0; connect these pins to the VDDD pin voltage (V_{DDD}) to set them to 1 (see Table 4).

Table 4: I²C Addresses

ADR1	ADR0	I²C Address
0	0	0x0070
0	1	0x0071
1	0	0x0072
1	1	0x0073

I²C Protocol

The I²C interface is a two-wire, bidirectional serial interface consisting of a data line (SDA) and a clock line (SCL). The lines are pulled to a bus voltage externally when they are idle.

The AXM8171A's interface is an I²C target that supports a maximum clock frequency up to 400kHz.

I²C Update Sequence

The AXM8171A requires a start command, valid I²C address, and data byte(s). After receiving each byte, the AXM8171A acknowledges the request by pulling the SDA line low during the high period of a single clock pulse.

Start and Stop Commands

The start and stop commands are signaled by the initiator device, and signify the beginning and the end of the I²C transfer, respectively. A start (S) command is defined as the SDA signal transitioning from high to low while SCL is high. A stop (P) command is defined as the SDA signal transitioning from low to high while SCL is high (see Figure 3).

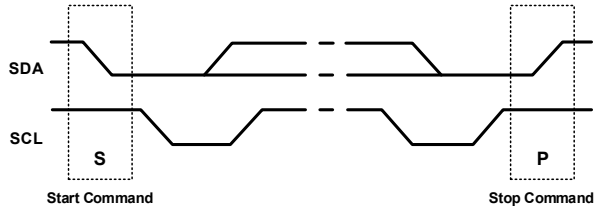

Figure 3: Start and Stop Commands

Address Byte

After the start command, the I²C initiator sends an address byte. The address byte consists of a 7-bit address field, and one bit (WR) that indicates if the transfer is a read (WR = 1) or a write (WR = 0).

The two least significant bits (LSBs) of the address, A0 and A1, are set by the ADR0 and ADR1 input pins. This means that a maximum of four devices can be connected to the same I²C bus.

The address byte is followed by an acknowledge (A) bit (see Figure 4).

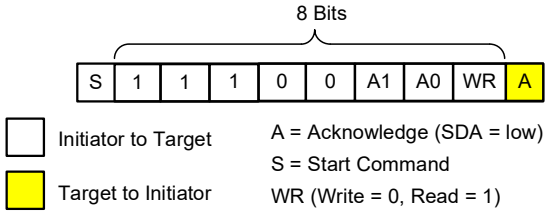

Figure 4: Address Byte

Data Bytes

After the address is acknowledged, 8-bit data bytes are sent, each followed by an acknowledge bit (see Figure 4). The state of the WR bit in the address byte determines if data is written from the initiator to the AXM8171A, or if data is read from the AXM8171A.

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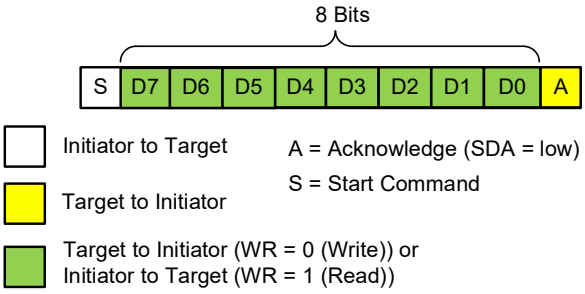

Figure 5: Data Byte

Communication Protocol

In addition to the I²C protocol, a specific protocol is implemented that allows for more complex control of the device compared to simple register/data write actions.

The communication protocol packets are composed of a transport header and a payload. The payload consists of a command ID and data. A command message that is divided into multiple packets is called a multi-packet command.

Figure 6 shows the I²C communication protocol.

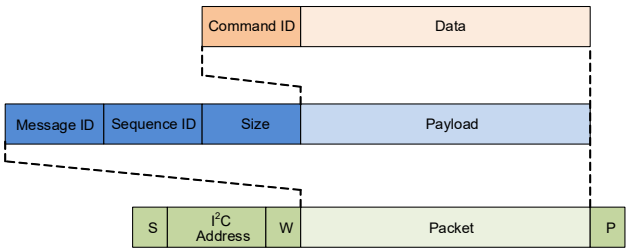

Figure 6: I²C Communication Protocol

Details about the available commands are described in a separate document available from Axign.

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APPLICATION INFORMATION

Power Supply

The AXM8171A-250 requires a 48V nominal power supply and a 3.3V control supply. The 48V supply requires a small external bulk capacitor. A minimum 220µF, 100V, low-impedance electrolytic capacitor is recommended. A 100µF capacitor is recommended for the 3.3V supply.

Output Load

The AXM8171A-250 can support output load impedances from 2Ω to infinity (open load) without impacting performance.

Similar to many audio amplifiers, connecting a highly capacitive load to the output can result in stability issues. It is recommended to limit the capacitance applied to the output to a maximum of 330nF.

Under-Voltage Protection (UVP)

The AXM8171-250 provides under-voltage protection (UVP) on both the VDDP and VDDD supply pins. The amplifier turns off when either of the supplies drops below its respective threshold. If either of the supplies exceeds the threshold, the amplifier resumes operation according to its previous state (on, off, or muted).

Over-Voltage Protection (OVP)

The AXM8171A-250 provides over-voltage protection (OVP) on the VDDP pin. If the OVP threshold is reached, the power stage is turned off in an attempt to protect the power stage. Supplying voltages exceeding the absolute maximum voltage may damage the device.

DC Protection

The AXM8171A-250 provides DC protection that shuts down the amplifier if the DC output level reaches the DC protection threshold for longer than 3 seconds. If DC protection is triggered, the amplifier remains in the protected/off state until the device enters either HW mode or SW mode, described below:

- HW mode: The user toggles the ON/OFF pin low, then high.
- SW mode: The user sends an off command, followed by an on command.

Over-Current Protection (OCP)

The AXM8171A-250 provides over-current protection (OCP). Once the current in either of the power stage's half-bridge exceeds the OCP limit, the amplifier turns off to protect it. The module attempts to restart after the restart time (t_{RES}).

Over-Temperature Protection (OTP)

The AXM8171-250 provides over-temperature protection (OTP). The amplifier turns off if the OTP threshold is reached. The module attempts to restart after t_{RES}.

Clock Failure Protection

The AXM8171A-250 provides clock failure protection. If a missing FCLK or BCLK is detected, the device turns off. Once both clocks are restored, the amplifier resumes operation according to its previous state (on, off, or muted).

There is no protection in the case of a misconfigured sample rate. For example, if the sample rate is configured as 96kHz but a 48kHz I2S/TDM stream is provided, the internal phase-locked loop (PLL) becomes locked and all frequencies are a factor 2 or lower. This can result in audible pops and clicks, and bad amplifier performance.

Turn-On Sequence

To turn on the AXM8171A-250 in HW mode, configure all the HW mode setting pins, then supply V_{DDD} and V_{DDP}. The order for turning on the supplies does not matter. Optionally pull the ON and MUTE pins high to turn on the amplifier module and unmute it, or simply connect the pins to V_{DDD}.

To turn on the AXM8171A-250 in SW mode, set the address pins to the correct value, then supply V_{DDD} and V_{DDP}. The order for turning on the supplies does not matter. Optionally send I^2C commands to configure the module. Lastly, send the I^2C commands to turn on and unmute the module. The commands are described in a separate document available from Axign.

Turn-Off Sequence

To turn off the AXM8171A-250, turn off V_{DDP} and ensure that V_{DDD} remains stable for at least 100ms after the VDDP pin voltage (V_{DDP}) drops below the under-voltage lockout (UVLO) level. This prevents unwanted pops and clicks during shutdown.

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PCB Mounting

The AXM8171A can be soldered directly into a PCB or mounted in a socket. The following are recommended sockets:

- CN1: Samtec FLE-111-01-G-DV-A-K-TR for an 11-pin, 2-row header, 1.27mm pitch female connector.
- 1.5mm pins: Mill-Max 0436-0-15-15-03-27-10-0 or equivalent for a 1.5mm pin PCB socket.

PCB Layout Guidelines

Efficient PCB layout is critical for stable audio module operation. For the best results, refer to Figure 7 and follow the guidelines below:

1. Place one or more minimum 220µF electrolytic capacitors close to the VDDP pins of the module, connected between VDDP and GND.
2. Place a minimum 100µF electrolytic capacitor between VDDD and GND.
3. It is recommended to route the I²S/TDM lines on an inner layer.

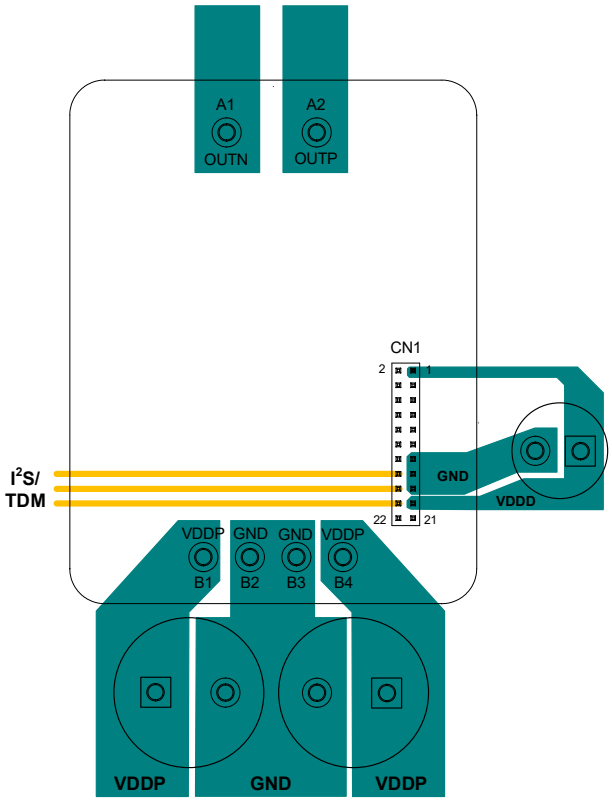

Figure 7: Recommended PCB Layout

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TYPICAL APPLICATION CIRCUIT

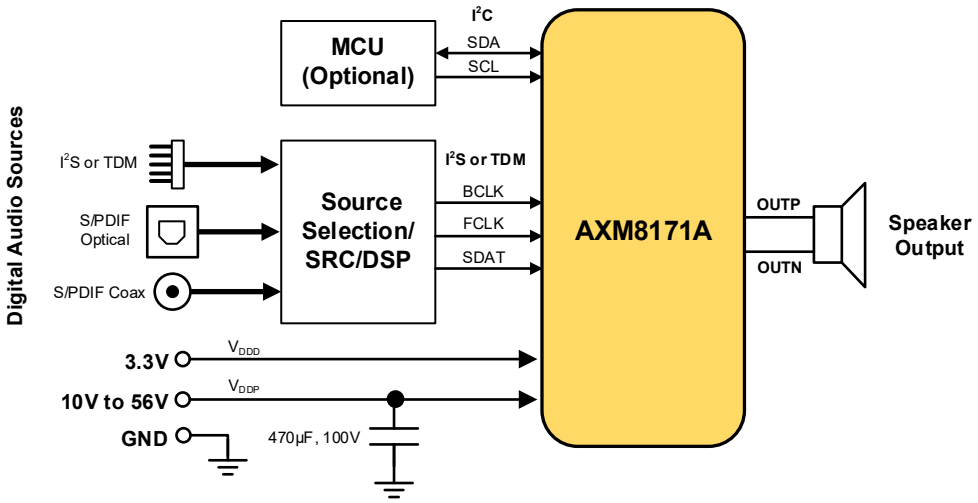

Figure 8: Typical Application Circuit

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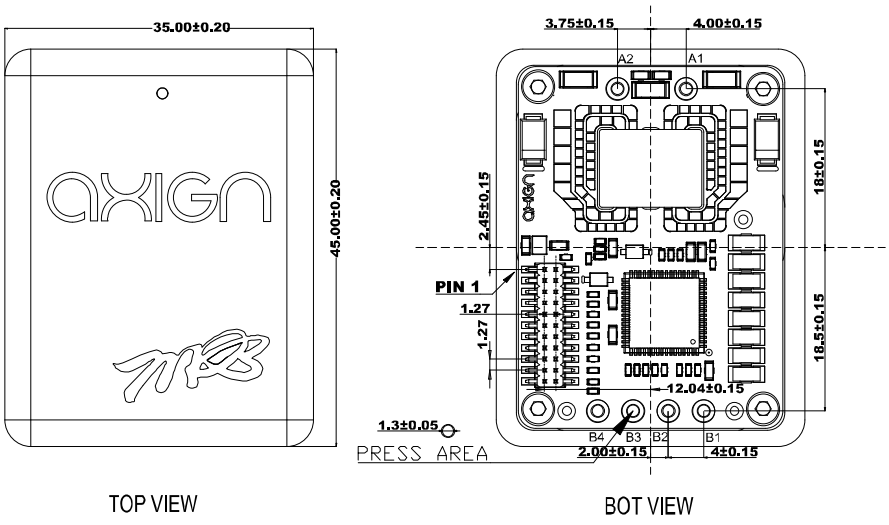
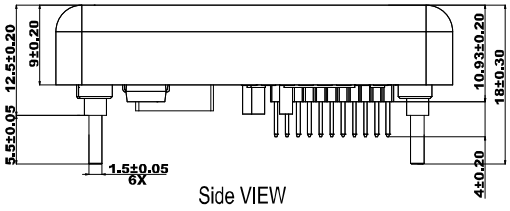
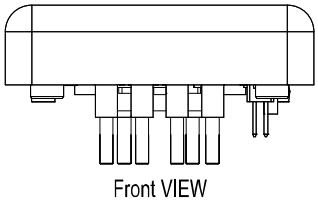
PACKAGE INFORMATION

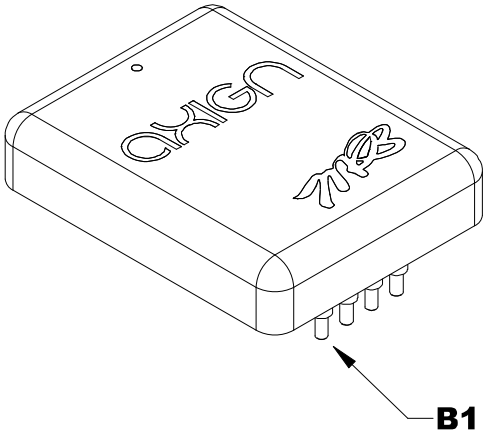
35mmx45mm

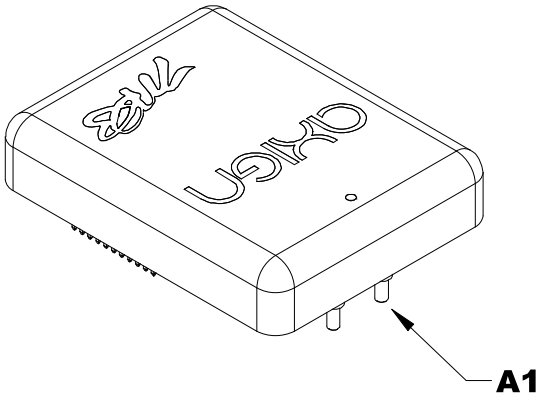


Pin #	Name
A1	OUTN
A2	OUTP
B1, B4	VDDP
B2, B3	GND









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REVISION HISTORY

Revision #	Revision Date	Description	Pages Updated
1.0	11/20/2026	Initial Release	-

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